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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,039	12/30/2003	Steven K. Reinhardt	42P17403	9187

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EXAMINER	
GEIB, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,039	REINHARDT ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
12/22/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/05/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 12/30/2003, Declaration on 06/24/2004, and Information Disclosure Statement on 04/05/2006.

Claim Objections

3. Claims 1-10 are objected to because of the following informalities:

Regarding claim 1:

The limitation "saving result from ... and result from" in lines 4-5 should be changed to "saving a result from ... and a result from".

The limitation "committing a single set of instruction" in line 7 should be changed to "committing a single set of instructions".

Regarding claim 2:

The limitation "wherein the saved result are saved" should be changed to "wherein the saved results are saved".

Regarding claim 3:

The second period at the end of the sentence should be deleted.

4. All claims objected to that have not been specifically addressed above are objected to on the basis of dependence.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 1 recites the limitation "saving [a] result from the instruction executed in the leading thread and [a] result from the instruction in the trailing thread" in lines 4-5 of the claim. As there is no previous mention of a specific instructions in the leading and trailing threads in the claim, there is insufficient antecedent basis for this limitation in the claim. The limitation "saving [a] result from the instruction executed in the leading thread and [a] result from the instruction in the trailing thread" will be interpreted as "saving [a] result from an instruction executed in the leading thread and [a] result from an instruction in the trailing thread" for the remainder of the examination as this appears to be what applicant intended.

8. Claims 4 and 8 recite the limitation "wherein the corresponding instructions read by the leading thread during the epoch". As there is no previous mention of corresponding instructions read by the leading thread during the epoch" in the claims, there is insufficient antecedent basis for this limitation in the claims. The limitation "wherein the corresponding instructions read by the leading thread during the epoch" will be interpreted as "wherein corresponding

instructions read by the leading thread during an epoch" for the remainder of the examination as this appears to be what applicant intended.

9. Claims 4 and 8 recite the limitation "when the corresponding trailing thread loads occurs". As there is no previous mention of corresponding trailing thread loads in the claims, there is insufficient antecedent basis for this limitation in the claims. The limitation "when the corresponding trailing thread loads occurs" will be interpreted as "when corresponding trailing thread loads occur" for the remainder of the examination as this appears to be what applicant intended.

10. Claim 5 recites the limitations "means for saving the executed threads in a memory" and "means for comparing the results saved in memory". The first of the above-mentioned limitation renders the claim indefinite as it is unclear to the examiner how an executed thread can be saved to memory. Regarding the second of the above-mentioned limitations, as there is no previous mention of results in the claim, there is insufficient antecedent basis for this limitation in the claim. In view of both of the above-mentioned limitations, the limitation "means for saving the executed threads in a memory" will be interpreted as "means for saving results from the executed threads in a memory" as this appears to be what applicant intended. The examiner notes that this interpretation provides antecedent basis for the limitation "means for comparing the results saved in memory".

11. Claim 5 recites the limitation "means for committing a single set of thread to a memory state". This limitation renders the claim indefinite as it is unclear to the examiner how a "set of thread" can committed to a memory state. The

limitation "means for committing a single set of thread to a memory state" will be interpreted as "means for committing a single set of instructions to a memory state" as this appears to be what applicant intended as indicated by a similar limitation in independent claim 1.

12. Claim 7 recites the limitation "wherein each epoch is executed twice". As there is no previous mention of epochs in the claim, there is insufficient antecedent basis for this limitation in the claim. The limitation "wherein each epoch is executed twice" will be interpreted as "wherein epochs are executed twice" for the remainder of the examination as this appears to be what applicant intended.

13. Claim 9 recites the limitation "wherein the buffered threads are stored as speculative". As there is no previous mention of buffered threads in the claim, there is insufficient antecedent basis for this limitation in the claim. The limitation "wherein the buffered threads are stored as speculative" will be interpreted as "wherein buffered threads are stored as speculative" for the remainder of the examination as this appears to be what applicant intended.

14. All claims rejected by 35 U.S.C. 112, second paragraph, that have not been specifically addressed above are rejected on the basis of dependence.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Vijaykumar et al., "Transient-Fault Recovery Using Simultaneous Multithreading" (Herein referred to as Vijaykumar).

17. Referring to claim 1, Vijaykumar has taught a method comprising:

executing corresponding instruction threads in parallel as a leading thread and a trailing thread *[see 2nd and 4th paragraphs of section 1]*;

saving a result from an instruction executed in the leading thread and a result from an instruction executed in the trailing thread to memory *[see 4th paragraph of section 3.3]*;

comparing the results saved in memory *[see 4th paragraph of section 3.3]*;

committing a single set of instruction to a memory state based on the compared result *[committing trailing thread stores in the commit vector; see 5th and 6th paragraphs of section 3.3]*; and

deferring external updates until completion of the step of committing *[stores to external memory are deferred unit the trailing stores commit; see 5th and 6th paragraphs of section 3.3]*.

18. Referring to claim 2, Vijaykumar has taught the method of claim 1, wherein the saved results are saved as speculative *[see 3rd paragraph of section 3]*.

19. Referring to claim 3, Vijaykumar has taught the method of claim 1 wherein the instructions are epoch instructions *[see 2nd and 4th paragraphs of section 1]*.

20. Referring to claim 4, Vijaykumar has taught the method of claim 3, wherein the corresponding instructions read by the leading thread during the epoch contains same value when the corresponding trailing thread loads occurs *[see 4th and 5th paragraphs of section 3.3]*.

21. Referring to claim 5, Vijaykumar has taught an apparatus comprising:

means for executing parallel threads as a leading thread and a trailing thread *[see 2nd and 4th paragraphs of section 1]*;

means for saving results from the executed threads in a memory *[see 4th paragraph of section 3.3]*;

means for comparing the results saved in memory *[see 4th paragraph of section 3.3]*;

means for committing a single set of instructions to a memory state based on the compared result *[committing trailing thread stores in the commit vector; see 5th and 6th paragraphs of section 3.3]*; and

means for deferring external updates until completion of the step of committing *[stores to external memory are deferred unit the trailing stores commit; see 5th and 6th paragraphs of section 3.3]*.

22. Referring to claim 6, Vijaykumar has taught the apparatus of claim 5 wherein the executed threads are epoch threads *[see 2nd and 4th paragraphs of section 1]*.

23. Referring to claim 7, Vijaykumar has taught the apparatus of claim 6, wherein epochs are executed twice *[by leading and trailing threads; see 2nd and 4th paragraphs of section 1]*.

24. Referring to claim 8, given the similarities between claim 4 and claim 8 the arguments as stated for the rejection of claim 4 also apply to claim 8.

25. Referring to claim 9, Vijaykumar has taught the apparatus of claim 8 wherein buffered threads are stored as speculative *[see 3rd paragraph of section 3]*.

26. Referring to claim 10, Vijaykumar has taught the apparatus of claim 9 wherein the single set is committed if the compare result matches *[see 4th and 5th paragraphs of section 3.3]*.

Conclusion

27. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sundaramoorthy et al., "Slipstream Processors: Improving both Performance and Fault Tolerance", has taught a method of executing redundant threads to improves performance and fault tolerance.

Gomaa et al., "Transient-Fault Recovery for Chip Multiprocessors", has taught a method of executing redundant threads and supporting fault recovery on a chip multiprocessor.

Quach, U.S. Patent No. 6,625,749, has taught a method of recovering from soft errors using redundant threads on a chip multiprocessor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

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12/22/2006